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10/539,196	06/17/2005	David R Evoy	US02 0617 US	2385
65913	7550	05/12/2009	EXAMINER	
NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			VAUGHAN, MICHAEL R	
			ART UNIT	PAPER NUMBER
			2431	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary

Application No.

10/539,196

Applicant(s)

EVOY, DAVID R

Examiner

MICHAEL R. VAUGHAN

Art Unit

2431

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 April 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 and 14-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 and 14-40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on **4/24/09** has been entered.

Claims 1, 2, 14-16, 18, 23, 26-35, and 37-40 have been amended. Claims 1-12 and 14-40 are pending.

Response to Amendment

Claim Objections

Claims 11 and 12 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. As per claim 11, it does not further limit the circuit arrangement of claim 2 by introducing an integrated

circuit. As per claim 12, it does not further limit the circuit arrangement of claim 2 or the integrated circuit of claim 11.

Claims 14, 23, and 32 are objected to because of the following informalities: the comma after "access control" should follow the preceding word "encrypted".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-12 and 14-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1, 2, 14, 15, 23, and 32, the new amendment being a wherein clause, seems to imply additional limitations added to functions preceding the clause. Implicit or not, the functions of access control and decoding are not defined or mentioned prior to this newly added clause. It is unclear what entity is performing the actual function. They seem to be performed on the integrated circuits, is it an undefined chip which exists in the circuit for performing the functionality? Also the notion of

decoding implies something was encoding previously? There is no step or logic defined to perform encoding. How did the data get encoded? What is being decoding?

As per claims 1, 2, 15, and 23, the phrase "separately performed" is indefinite. First of all for the reasons mention above, the actual access control and decoding is ambiguous. In this case, does separately mean a) the access control and decoding are separate from the encryption of data sent over the channel or b) the access control is separate from the decoding? If b) is the case, it is still unclear which integrated circuit (first or second) performs which function.

As per claim 11 and 12, it is unclear what is being claimed. The claims being dependent claims, reference their parent claims have been written in an independent form. If Applicant wishes to claim a new entity (circuit) in claim 11 it should be written in independent form explicitly including the desired limitation. Claim 12 claims a system dependent on a circuit further dependent on a system. Appropriate correction is required.

As per claims 4, 7, 8, and 18, data appears to be defined for a second time. Therefore it is unclear whether this data is something new or refers to data already defined. For example in claim 4, data is outputted. In claim 2, data is already defined. Are they the same?

Throughout the claims, the word data is used in defining both the information that flows over both the default channel and the encrypted channel. This can be confusing and misleading especially when the hardware encryption circuit is configured to encrypt "all data". The invention would be clearer if the claims simply conveyed that all data is

encrypted and it flows over the dedicated encrypted virtual channel and definitively distinguishes this data from what flows over the default virtual channel.

As per claim 15, "two integrated circuits" are rendered indefinite because only a first integrated circuit is defined. So it is unclear where this is two new circuits or only on additional circuit.

Response to Arguments

Applicant's arguments filed 4/24/09 have been fully considered but they are not persuasive. First of all, with the above stated indefiniteness relating to the newly amended claims it is difficult to ascertain the meaning and scope by which the new amendments encompass. Applicant has argued that the prior art of record does not teach sending all encrypted data over a virtual channel which seems to correspond to the first part of the new limitations. The primary reference Ishiguro teaches encrypted all data sent between two apparatus are encrypted (page 2, line 40). Ishiguro is not concerned with data which is not encrypted. In the real-time data transmission system of Abbott, it is taught that dedicated channels can be implemented in order to decrease latency. This is useful when transmitting audio and video. Abbott teaches using a dedicated channel other than the main data delivery channel to send protocol messages back and forth (col. 8, lines 60-65). Examiner has relied upon this teaching in conjunction with Ishiguro's system of sending encrypted data. Combined, the encrypted data would still be encrypted along its own dedicated virtual channel and a separated virtual channel would be used for messaging and protocol overhead. It would have

been obvious to combine these two references when wanting to encrypt real-time data streams.

With respect to the notion that the prior art does not teach access control and decoding, Examiner is not giving any patentable weight to those features because it is unclear what they do and how they are coupled to the rest of the invention. Examiner will reserve interpretation of the prior art until it is known how these functions operate within the scope of the claimed invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-12, 14-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishiguro et al. (EP 0,875,813 A2) in view of Paskins et al. (EP 0,952,733 A2), Mowery et al. (US 2003/0081391 A1), and Abbott et al. (US6,141,324).

With respect to claim 1, Ishiguro teaches the limitation of "a first integrated circuit, the first integrated circuit including a first logic block configured to generate a data stream" (Fig. 3 and 10; page 6, line 19) as the firmware that transmits data to personal computer.

In addition, Ishiguro teaches the limitation of "a first integrated circuit, the first integrated circuit including a hardware encryption circuit coupled to the first logic block and configured to encrypt the data stream to generate an encrypted data stream" (Fig. 3 and 10; page 2, lines 36-37) as enciphering means for enciphering data.

Additionally, Ishiguro teaches the limitations of "a second PCI- Express-compatible interface circuit coupled to the PCI-Express-compatible interconnect to receive the encrypted data stream over the dedicated encrypted virtual channel, the second PCI-Express-compatible interface including a plurality of channel interconnects, each associated with a virtual channel among the plurality of virtual channels" and "a hardware decryption circuit coupled to a first channel interconnect among the plurality of channel interconnects for the second PCI-Express-compatible interface circuit and configured to decrypt the encrypted data stream" (Fig. 3 and 10; page 2, lines 47-48) as receiving means for receiving enciphered data and deciphering means for deciphering data.

Further, Ishiguro teaches the limitation of "a second logic block coupled to the hardware decryption circuit and configured to use the decrypted data stream" (Fig. 3 and 10).

Finally, Ishiguro teaches the limitation of "control logic coupled to at least one of the first and second PCI-Express- compatible interface circuits and configured to communicate authorization data over the default virtual channel to authorize secure communication between the first and second integrated circuits over the dedicated encrypted virtual channel" (Fig. 3; page 5, lines 19-22) as firmware and a license

manager carrying out the authentication procedure between one of software programs stored in the ROM of the DVD and one of software programs stored in the ROM of the personal computer.

It is noted, however, that Ishiguro does not explicitly teach the limitations of "a PCI-Express-compatible interface circuit configured to support data communication over a plurality of PCI-Express virtual channels", "wherein the first PCI-Express-compatible interface circuit includes a plurality of channel interconnects, each associated with a virtual channel among the plurality of virtual channels", "wherein a first channel interconnect among the plurality of virtual channels is coupled to the hardware encryption circuit to receive the encrypted data stream", and "wherein the first PCI-Express-compatible interface circuit is configured to communicate the encrypted data stream from the hardware encryption circuit over the dedicated encrypted virtual channel."

On the other hand, Ishiguro teaches that the interconnection for the elements of his invention is provided through the 1394 bus through 1394 interface (page 4, lines 47-48).

In addition, Paskins teaches a transport stream interface in which various virtual channels are time-multiplexed (column 1, paragraph 0003) which is implemented on IEEE 1394 Serial Bus (Abstract).

It is further noted that neither Ishiguro nor Paskins teach the limitation of "PCI-Express-compatible interface circuit."

However, Mowery teaches this limitation (page 2, paragraph 0023) as the present invention is operable with other technical standards. For example, rather than USB or USB 2.0, the present invention is also operable with Institute of Electrical and Electronics Engineers (IEEE) 1394 (FireWire), Ethernet, and serial and parallel communications ports, peripheral components interconnect (PCI), PCI-X, and PCI-Express to list a few.

Furthermore, it is noted that Ishiguro does not explicitly teach the limitation of "the plurality of PCI-Express virtual channels includes an unencrypted default virtual channel and a dedicated encrypted virtual channel configured to communicate encrypted data exclusively"

On the other hand, Abbott teaches the abovementioned limitation (Fig. 4; column 8, line 61 – column 9, line 1) as all communications between the modems can be implemented in a dedicated communication channel. This dedicated communication channel can be a dedicated virtual channel, or a dedicated physical channel.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to incorporate teachings Paskins into the system of Ishiguro to provide a higher throughput by multiplexing plurality of channels. Further, it would also be obvious to incorporate teachings of Mowery into the system of Ishiguro and Paskins to provide greater bandwidth and decrease in power consumption. Furthermore, it would have been obvious to one of the ordinary skill in the art to incorporate teachings of Abbott into the system of Ishiguro, Paskins, and Mowery because it would provide a secure channel for real-time data transfer over a well-known bus architecture (PCI-X).

Claims 2-4, 9-12, and 14 are rejected in view of the same reasons stated in the rejection of independent claim 1.

With respect to claims 5-8, Paskins teaches a transport stream interface in which various virtual channels are time-multiplexed (column 1, paragraph 0003) which is implemented on IEEE 1394 Serial Bus (Abstract) that can be used for the throughput control of the system. In addition, Abbott teaches the limitation of dedicated virtual communication channel (Fig. 4; column 8, line 61 – column 9, line 1) that can be used to ensure the security of the data transfers.

Claim 14 are rejected in view of the same reasons stated in the rejection of independent claim 1.

With respect to claims 15-17 and 20-22, they are rejected in view of the same reasons as stated in the rejection of independent claim 1.

With respect to claims 18 and 19, they are rejected in view of the same reasons as stated in the rejection of claims 5-8.

Claims 23-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishiguro et al. (EP 0,875,813 A2) in view of Paskins et al. (EP 0,952,733 A2), and further in view of Abbott et al. (US6,141,324).

With respect to claim 23, Ishiguro teaches the limitation of "re-encrypting the first decrypted data stream in the first integrated circuit to generate a second encrypted data stream" (Fig. 3 and 10; page 2, lines 36-37) as enciphering means for enciphering data.

In addition, Ishiguro teaches the limitation of "communicating the second encrypted data stream from the first integrated circuit to a second integrated circuit" (Fig. 3 and 10; page 6, line 19) as the firmware that transmits data to personal computer.

Finally, Ishiguro teaches the limitation of "decrypting the second encrypted data stream in the second integrated circuit to generate a second decrypted data stream" (Fig. 3 and 10; page 2, lines 47-48) as receiving means for receiving enciphered data and deciphering means for deciphering data.

It is noted however, that Ishiguro does not explicitly teach the limitations of "decrypting a first encrypted data stream in a first integrated circuit to generate a first decrypted data stream", "a multi-channel serial interconnect to which the first and second integrated circuits are connected", and "a dedicated encrypted virtual channel among a plurality of virtual channels supported by the multi-channel serial interconnect".

On the other hand, Paskins teaches the limitation of "decrypting a first encrypted data stream in a first integrated circuit to generate a first decrypted data stream" (Fig. 1) as a path that goes through Demodulator 16, Descrambler 18, and Demultiplexer 20.

In addition, Paskins teaches the limitation of "a multi-channel serial interconnect to which the first and second integrated circuits are connected" (column 1, paragraph 0003) as a transport stream interface in which various virtual channels are time-multiplexed, which is implemented on IEEE 1394 Serial Bus (Abstract).

In addition, Abbott teaches the limitation of "a dedicated encrypted virtual channel among a plurality of virtual channels supported by the multi-channel serial interconnect" (Fig. 4; column 8, line 61 – column 9, line 1) as all communications between the modems can be implemented in a dedicated communication channel. This dedicated communication channel can be a dedicated virtual channel, or a dedicated physical channel.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to incorporate teachings Paskins into the system of Ishiguro to provide a higher throughput by multiplexing plurality of channels. Further, it would have been obvious to one of the ordinary skill in the art to incorporate teachings of Abbott into the system of Ishiguro and Paskins because it would provide a secure channel for real-time data transfer.

With respect to claim 24, Paskins teaches the limitation of "demodulating a modulated input signal to generate the first encrypted data stream" (Fig. 1) as demodulator 16.

With respect to claims 25 and 26, Paskins teaches the limitation of "decoding the second decrypted data stream in the second integrated circuit to generate a decoded data stream" and "wherein the modulated input signal comprises a satellite broadcast signal, wherein the first encrypted data stream comprises an encrypted MPEG data stream, and wherein decoding the second decrypted data stream in the second integrated circuit comprises performing MPEG decoding on the second decrypted data stream" (Fig. 1) as MPEG Decoder.

With respect to claim 27, it is noted that neither of Ishiguro, Paskins and Abbott teach the limitation of "performing regional access control on the first encrypted data stream."

However, examiner takes the official notice that using the regional encoding to protect the data distributed on DVDs is well known in the art. Therefore, it would have been obvious to one of the ordinary skill in the art at the time of the invention to use such a technique to access data distributed on DVD.

With respect to claim 28, Ishiguro teaches the limitation of "performing subscriber access control on the first encrypted data stream" (Fig. 3; page 5, lines 19-22) as firmware and a license manager carrying out the authentication procedure between one of software programs stored in the ROM of the DVD and one of software programs stored in the ROM of the personal computer.

With respect to claim 29, Paskins teaches the limitation of "the first and second integrated circuits are disposed in a set top box" (Fig. 6; column 16, paragraph 0118) as a device such as a host receiver or Conditional Access Module implementing a Command Interface over an IEEE 1394 Serial Bus.

With respect to claim 30, Paskins teaches the limitation of "the first integrated circuit is disposed on an access card coupled to the second integrated circuit via a connector" (column 10, lines 41-44) as the DVB Common Interface has been designed with a layered architecture to allow new physical layers (for example the smart card form factor).

With respect to claim 31, it is rejected in view of the same reasons stated in the rejection of independent claim 23.

With respect to claims 32-40, they are rejected in view of the same reasons stated in the rejection of claims 23-31.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL R. VAUGHAN whose telephone number is (571)270-7316. The examiner can normally be reached on Monday - Thursday, 7:30am

- 5:00pm, EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. R. V./

Examiner, Art Unit 2431

/Ayaz R. Sheikh/
Supervisory Patent Examiner, Art Unit 2431